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**UTILITY
PATENT APPLICATION
TRANSMITTAL**

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. **MI22-1330**First Inventor or Application Identifier **Gar0 J. Derderian**Title **Capacitor Fabrication Methods and Capacitor Construction**Express Mail Label No. **EL465688219US****APPLICATION ELEMENTS**

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 202311. ☒ * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)2. ☒ Specification [Total Pages **28**]
(preferred arrangement set forth below)

- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets **5**]4. Oath or Declaration [Total Pages **1**]

- a. ☐ Newly executed (original or copy)
- b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
 - i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting
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*** NOTE FOR ITEMS 1 & 3 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY
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ACCOMPANYING APPLICATION PARTS7. ☐ Assignment Papers (cover sheet & document(s))8. ☐ 37 C.F.R. § 3.73(b) Statement ☐ Power of
(when there is an assignee) ☐ Attorney9. ☐ English Translation Document (if applicable)10. ☐ Information Disclosure ☐ Copies of IDS
Statement (IDS)/PTO-1449 ☐ Citations11. ☐ Preliminary Amendment12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)13. ☐ * Small Entity ☐ Statement filed in prior application
Statement(s) ☐ Status still proper and desired
(PTO/SB/09-12)14. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)15. ☒ Other: **Check in the amount of \$1002.00**16. If a **CONTINUING APPLICATION**, check appropriate box, and supply the requisite information below and in a preliminary amendment:☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP)

of prior application No: _____ / _____

Prior application information: Examiner _____

Group / Art Unit: _____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.**17. CORRESPONDENCE ADDRESS**☒ Customer Number or Bar Code Label**021567**or ☐ Correspondence address below

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Name (Print/Type)

James E. Lake

Registration No. (Attorney/Agent)

44,854

Signature

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TOTAL AMOUNT OF PAYMENT (\$1002.00)

Complete if Known

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| Application Number | Unknown |
| Filing Date | August 31, 2000 |
| First Named Inventor | Garo J. Derderian |
| Examiner Name | Unassigned |
| Group / Art Unit | Unassigned |
| Attorney Docket No. | MI22-1330 |

METHOD OF PAYMENT (check one)

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Wells, St. John

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FEE CALCULATION

1. BASIC FILING FEE

| Large Entity Fee Code | Small Entity Fee Code | Fee Description | Fee Paid |
|-----------------------|-----------------------|------------------------|----------|
| 101 760 | 201 380 | Utility filing fee | 690.00 |
| 106 310 | 206 155 | Design filing fee | |
| 107 480 | 207 240 | Plant filing fee | |
| 108 760 | 208 380 | Reissue filing fee | |
| 114 150 | 214 75 | Provisional filing fee | |

SUBTOTAL (1) (\$) 690.00

2. EXTRA CLAIM FEES

| Total Claims | Extra Claims | Fee from below | Fee Paid |
|--------------------|--------------|----------------|----------|
| 33 | -20** = 13 | 18.00 | 234.00 |
| Independent Claims | 4 | -3** = 1 | 78.00 |
| Multiple Dependent | | | 0.00 |

**or number previously paid, if greater; For Reissues, see below

| Large Entity Fee Code | Small Entity Fee Code | Fee Description |
|-----------------------|-----------------------|--|
| 103 18 | 203 9 | Claims in excess of 20 |
| 102 78 | 202 39 | Independent claims in excess of 3 |
| 104 260 | 204 130 | Multiple dependent claim, if not paid |
| 109 78 | 209 39 | ** Reissue independent claims over original patent |
| 110 18 | 210 9 | ** Reissue claims in excess of 20 and over original patent |

SUBTOTAL (2) (\$) 312.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

| Large Entity Fee Code | Small Entity Fee Code | Fee Description | Fee Paid |
|-----------------------|-----------------------|--|----------|
| 105 130 | 205 65 | Surcharge - late filing fee or oath | 0.00 |
| 127 50 | 227 25 | Surcharge - late provisional filing fee or cover sheet. | 0.00 |
| 139 130 | 139 130 | Non-English specification | 0.00 |
| 147 2,520 | 147 2,520 | For filing a request for reexamination | 0.00 |
| 112 920* | 112 920* | Requesting publication of SIR prior to Examiner action | 0.00 |
| 113 1,840* | 113 1,840* | Requesting publication of SIR after Examiner action | 0.00 |
| 115 110 | 215 55 | Extension for reply within first month | 0.00 |
| 116 380 | 216 190 | Extension for reply within second month | 0.00 |
| 117 870 | 217 435 | Extension for reply within third month | 0.00 |
| 118 1,360 | 218 680 | Extension for reply within fourth month | 0.00 |
| 128 1,850 | 228 925 | Extension for reply within fifth month | 0.00 |
| 119 300 | 219 150 | Notice of Appeal | 0.00 |
| 120 300 | 220 150 | Filing a brief in support of an appeal | 0.00 |
| 121 260 | 221 130 | Request for oral hearing | 0.00 |
| 138 1,510 | 138 1,510 | Petition to institute a public use proceeding | 0.00 |
| 140 110 | 240 55 | Petition to revive - unavoidable | 0.00 |
| 141 1,210 | 241 605 | Petition to revive - unintentional | 0.00 |
| 142 1,210 | 242 605 | Utility issue fee (or reissue) | 0.00 |
| 143 430 | 243 215 | Design issue fee | 0.00 |
| 144 580 | 244 290 | Plant issue fee | 0.00 |
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| 123 50 | 123 50 | Petitions related to provisional applications | 0.00 |
| 126 240 | 126 240 | Submission of Information Disclosure Stmt | 0.00 |
| 581 40 | 581 40 | Recording each patent assignment per property (times number of properties) | 0.00 |
| 146 760 | 246 380 | Filing a submission after final rejection (37 CFR 1.129(a)) | 0.00 |
| 149 760 | 249 380 | For each additional invention to be examined (37 CFR 1.129(b)) | 0.00 |
| Other fee (specify) | | | 0.00 |
| Other fee (specify) | | | 0.00 |

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Typed or Printed Name James E. Lake

Signature

[Signature]

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EL465688219US

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

CAPACITOR FABRICATION METHODS AND CAPACITOR CONSTRUCTIONS

* * * * *

INVENTORS

Garro J. Derderian
Gurtej S. Sandhu

ATTORNEY'S DOCKET NO. MI22-1330

CAPACITOR FABRICATION METHODS AND CAPACITOR CONSTRUCTIONS

TECHNICAL FIELD

The aspects of the invention relate to capacitor fabrication methods including forming conductive barrier layers and capacitor constructions having conductive barrier layers.

BACKGROUND OF THE INVENTION

Capacitors are common devices used in electronics, such as integrated circuits, and particularly semiconductor-based technologies. Two common capacitor structures include metal-insulator-metal (MIM) capacitors and metal-insulator-semiconductor (MIS) capacitors. One important factor to consider when selecting a capacitor structure may be the capacitance per unit area. MIS capacitors may be advantageous since a first electrode as the semiconductor may be formed of hemispherical grain (HSG) polysilicon that exhibits a higher surface area in a given region compared to a planar surface of amorphous silicon. The higher surface area provides more capacitance per unit area occupied by a capacitor.

However, a high K factor (also known as dielectric constant or "κ") dielectric material may be desirable to further enhance capacitance. Ta₂O₅ is one example of a high K factor dielectric, but it inherently forms an interfacial dielectric layer of SiO₂ when formed on a capacitor

1 electrode comprising HSG. The interfacial dielectric exhibits a lower K
2 factor than Ta₂O₅ and thus reduces the effective dielectric constant for
3 the capacitor construction. Such reduction may be significant enough to
4 eliminate any gain in capacitance per unit area otherwise achieved by
5 using HSG instead of a planar electrode. Use of other oxygen
6 containing high K dielectric materials has proved to create similar
7 problems.

8 Because it may be desirable to provide area enhancement of an
9 electrode in a MIM structure using HSG, one attempt at addressing the
10 stated problem is forming a silicon nitride insulative barrier layer over
11 the HSG. The silicon nitride barrier layer may be formed by nitridizing
12 the silicon of the outer surface of HSG. Unfortunately, silicon nitride
13 exhibits a K factor of only about 7, less than the K factor of some high
14 K factor dielectrics that are desirable. Accordingly, even the silicon
15 nitride barrier layer reduces the effective dielectric constant of the
16 capacitor.

SUMMARY OF THE INVENTION

In one aspect of the invention, a capacitor fabrication method may include forming a first capacitor electrode over a substrate and atomic layer depositing a conductive barrier layer to oxygen diffusion over the first electrode. A capacitor dielectric layer may be formed over the first electrode and a second capacitor electrode may be formed over the dielectric layer.

Another aspect of the invention may include chemisorbing a layer of a first precursor at least one monolayer thick over the first electrode and chemisorbing a layer of a second precursor at least one monolayer thick on the first precursor layer, a chemisorption product of the first and second precursor layers being comprised by a layer of a conductive barrier material.

Also, in another aspect of the invention a capacitor fabrication method may include forming a first capacitor electrode over a substrate. The first electrode can have an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate. A capacitor dielectric layer may be formed over the first electrode and a second capacitor electrode may be formed over the dielectric layer.

A still further aspect includes a capacitor fabrication method of forming an opening in an insulative layer over a substrate, the opening having sides and a bottom, forming a layer of polysilicon over the sides

1 and bottom of the opening, and removing the polysilicon layer from over
2 the bottom of the opening. At least some of the polysilicon layer may
3 be converted to hemispherical grain polysilicon. A first capacitor
4 electrode may be conformally formed on the converted polysilicon, the
5 first electrode being sufficiently thin that the first electrode has an outer
6 surface area per unit area greater than an outer surface area per unit
7 area of the substrate underlying the first electrode. A capacitor
8 dielectric layer may be formed over the first electrode and a second
9 capacitor electrode may be formed over the dielectric layer.

10 Other aspects of the invention include the capacitor constructions
11 formed from the above described methods.

12 13 14 **BRIEF DESCRIPTION OF THE DRAWINGS**

15 Preferred embodiments of the invention are described below with
16 reference to the following accompanying drawings.

17 Fig. 1 is an enlarged view of a section of a semiconductor wafer
18 at one processing step in accordance with the invention.

19 Fig. 2 is an enlarged view of the section of the Fig. 1 wafer at
20 a processing step subsequent to that depicted by Fig. 1.

21 Fig. 3 is an enlarged view of the section of the Fig. 1 wafer at
22 a processing step subsequent to that depicted by Fig. 2.
23

Fig. 4 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 3.

Fig. 5 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 4.

Fig. 6 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 5.

Fig. 7 is an enlarged view of the section of the Fig. 1 wafer at an alternate embodiment processing step subsequent to that depicted by Fig. 2 in accordance with alternate aspects of the invention.

Fig. 8 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 7.

Fig. 9 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 8.

Fig. 10 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 9.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Atomic layer deposition (ALD) involves formation of successive atomic layers on a substrate. Such layers may comprise an epitaxial, polycrystalline, amorphous, etc. material. ALD may also be referred to

1 as atomic layer epitaxy, atomic layer processing, etc. Further, the
2 invention may encompass other deposition methods not traditionally
3 referred to as ALD, for example, chemical vapor deposition (CVD), but
4 nevertheless including the method steps described herein. The deposition
5 methods herein may be described in the context of formation on a
6 semiconductor wafer. However, the invention encompasses deposition on
7 a variety of substrates besides semiconductor substrates.

8 In the context of this document, the term "semiconductor
9 substrate" or "semiconductive substrate" is defined to mean any
10 construction comprising semiconductive material, including, but not limited
11 to, bulk semiconductive materials such as a semiconductive wafer (either
12 alone or in assemblies comprising other materials thereon), and
13 semiconductive material layers (either alone or in assemblies comprising
14 other materials). The term "substrate" refers to any supporting
15 structure, including, but not limited to, the semiconductive substrates
16 described above.

17 Described in summary, ALD includes exposing an initial substrate
18 to a first chemical species to accomplish chemisorption of the species
19 onto the substrate. Theoretically, the chemisorption forms a monolayer
20 that is uniformly one atom or molecule thick on the entire exposed
21 initial substrate. In other words, a saturated monolayer. Practically, as
22 further described below, chemisorption might not occur on all portions
23 of the substrate. Nevertheless, such an imperfect monolayer is still a

monolayer in the context of this document. In many applications, merely a substantially saturated monolayer may be suitable. A substantially saturated monolayer is one that will still yield a deposited layer exhibiting the quality and/or properties desired for such layer.

The first species is purged from over the substrate and a second chemical species is provided to chemisorb onto the first monolayer of the first species. The second species is then purged and the steps are repeated with exposure of the second species monolayer to the first species. In some cases, the two monolayers may be of the same species. Also, a third species or more may be successively chemisorbed and purged just as described for the first and second species.

Purging may involve a variety of techniques including, but not limited to, contacting the substrate and/or monolayer with a carrier gas and/or lowering pressure to below the deposition pressure to reduce the concentration of a species contacting the substrate and/or chemisorbed species. Examples of carrier gases include N₂, Ar, He, Kr, Ne, Xe, etc. Purging may instead include contacting the substrate and/or monolayer with any substance that allows chemisorption byproducts to desorb and reduces the concentration of a contacting species preparatory to introducing another species. A suitable amount of purging can be determined experimentally as known to those skilled in the art. Purging time may be successively reduced to a purge time that yields an increase in film growth rate. The increase in film growth rate might be an

1 indication of a change to a non-ALD process regime and may be used
2 to establish a purge time limit.

3 ALD is often described as a self-limiting process, in that a finite
4 number of sites exist on a substrate to which the first species may form
5 chemical bonds. The second species might only bond to the first species
6 and thus may also be self-limiting. Once all of the finite number of
7 sites on a substrate are bonded with a first species, the first species will
8 often not bond to other of the first species already bonded with the
9 substrate. However, process conditions can be varied in ALD to
10 promote such bonding and render ALD not self-limiting. Accordingly,
11 ALD may also encompass a species forming other than one monolayer
12 at a time by stacking of a species, forming a layer more than one atom
13 or molecule thick. The various aspects of the present invention
14 described herein are applicable to any circumstance where ALD may be
15 desired.

16 Often, traditional ALD occurs within an often-used range of
17 temperature and pressure and according to established purging criteria
18 to achieve the desired formation of an overall ALD layer one monolayer
19 at a time. Even so, ALD conditions can vary greatly depending on the
20 particular precursors, layer composition, deposition equipment, and other
21 factors according to criteria known by those skilled in the art.
22 Maintaining the traditional conditions of temperature, pressure, and
23 purging minimizes unwanted reactions that may impact monolayer

1 formation and quality of the resulting overall ALD layer. Accordingly,
2 operating outside the traditional temperature and pressure ranges may
3 risk formation of defective monolayers.

4 The general technology of chemical vapor deposition (CVD)
5 includes a variety of more specific processes, including, but not limited
6 to, plasma enhanced CVD and others. CVD is commonly used to form
7 non-selectively a complete, deposited material on a substrate. One
8 characteristic of CVD is the simultaneous presence of multiple species
9 in the deposition chamber that react to form the deposited material.
10 Such condition is contrasted with the purging criteria for traditional ALD
11 wherein a substrate is contacted with a single deposition species that
12 chemisorbs to a substrate or previously deposited species. An ALD
13 process regime may provide a simultaneously contacted plurality of
14 species of a type or under conditions such that ALD chemisorption,
15 rather than CVD reaction occurs. Instead of reacting together, the
16 species may chemisorb to a substrate or previously deposited species,
17 providing a surface onto which subsequent species may next chemisorb
18 to form a complete layer of desired material. Under most CVD
19 conditions, deposition occurs largely independent of the composition or
20 surface properties of an underlying substrate. By contrast, chemisorption
21 rate in ALD might be influenced by the composition, crystalline
22 structure, and other properties of a substrate or chemisorbed species.
23

1 Other process conditions, for example, pressure and temperature, may
2 also influence chemisorption rate.

3 ALD, as well as other deposition methods and/or methods of
4 forming conductive barrier layers may be useful in capacitor fabrication
5 methods. According to one aspect of the invention, a capacitor
6 fabrication method includes forming a first capacitor electrode over a
7 substrate and atomic layer depositing a conductive barrier layer to oxygen
8 diffusion over the first electrode. A capacitor dielectric layer may be
9 formed over the first electrode and a second capacitor electrode may be
10 formed over the dielectric layer. At least one of the first or second
11 capacitor electrodes may comprise polysilicon, preferably hemispherical
12 grain (HSG) polysilicon. The dielectric layer may comprise oxygen.
13 Exemplary materials for the dielectric layer include, but are not limited
14 to, Ta_2O_5 , ZrO_2 , WO_3 , Al_2O_3 , HfO_2 , barium strontium titanate (BST), or
15 strontium titanate (ST).

16 Notably, the conductive barrier layer to oxygen diffusion formed
17 over the first electrode may provide the advantage of reducing oxidation
18 of the electrode by oxygen diffusion from an oxygen source, for example,
19 the dielectric layer. The dielectric layer may be formed over the barrier
20 layer, thus, the barrier layer may reduce oxygen diffusion to the first
21 capacitor electrode. Alternatively, such a barrier layer may reduce
22 oxygen diffusion from the first capacitor electrode or under the first
23 capacitor electrode to the dielectric layer or second capacitor electrode.

1 It follows then that the barrier layer may also be formed over the
2 capacitor dielectric layer with the second capacitor electrode over the
3 barrier layer such that the barrier layer reduces oxygen diffusion from
4 the dielectric layer to the second electrode. Such positioning may also
5 reduce oxygen diffusion from over the dielectric layer to the first
6 capacitor electrode, for example, oxygen diffusion from the second
7 capacitor electrode. Accordingly, one aspect of the invention may
8 include atomic layer depositing the barrier layer over the first electrode,
9 forming the dielectric layer over the barrier layer, and atomic layer
10 depositing another conductive barrier to oxygen diffusion over the
11 dielectric layer.

12 Prior to the atomic layer depositing, it may be advantageous to
13 clean the deposition substrate, for example, the first electrode. Cleaning
14 may be accomplished by a method comprising HF dip, HF vapor clean,
15 or NF_3 remote plasma. Such cleaning methods may be performed in
16 keeping with the knowledge of those skilled in the art. Likewise,
17 forming the first and second electrodes and dielectric layer may be
18 accomplished by methods known to those skilled in the art and may
19 include atomic layer deposition, but preferably other methods.

20 The atomic layer depositing of the barrier layer may occur at a
21 temperature of from about 100 to about 600 °C and at a pressure of
22 from about 0.1 to about 10 Torr. The dielectric layer may exhibit a K
23 factor of greater than about 7 at 20 °C. Examples of suitable materials

1 for the barrier layer include WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys,
2 Ir, Ir alloys, Pd, Pd alloys, RuO_x, or IrO_x, as well as other materials.
3 The barrier layer may have a thickness of from about 50 to about 500
4 Angstroms or another thickness depending on the material properties.

5 One consideration in selecting a material for the barrier layer is
6 the thickness and density of the barrier layer that will be sufficient to
7 achieve a desired level of oxygen diffusion reduction. Another factor to
8 evaluate is that the barrier layer might be considered to form a part of
9 a capacitor electrode when the barrier layer contacts one of the first or
10 second electrodes since the barrier layer is conductive. Accordingly, it
11 may be advantageous to recalculate the desired dimensions of an
12 electrode contacted by the barrier layer accounting for the presence of
13 the additional conductive material. Accordingly, a "conductive" material
14 as the term is used herein designates a material exhibiting a conductivity
15 at 20°C of greater than 10⁴ microOhm⁻¹ centimeter⁻¹, or preferably
16 greater than about 10¹² microOhm⁻¹ centimeter⁻¹. Notably, such definition
17 expressly includes "semiconductive" material in the range of about 10⁴
18 to about 10¹² microOhm⁻¹ centimeter⁻¹. As an alternative, a "conductive"
19 material in the present context might be viewed as a material that does
20 not substantially impact the capacitance otherwise achieved without the
21 material. Generally, an "insulative" material might produce a change in
22 capacitance as such a barrier layer.

1 As another aspect of the present invention, a capacitor fabrication
2 method may include forming a first capacitor electrode over a substrate,
3 chemisorbing a layer of a first precursor at least one monolayer thick
4 over the first electrode, and chemisorbing a layer of a second precursor
5 at least one monolayer thick on the first precursor layer. A
6 chemisorption product of the first and second precursor layers may be
7 comprised by a layer of a conductive barrier material. Because the
8 chemisorption product is comprised by the barrier layer, the barrier layer
9 may also include conductive barrier material that is not a chemisorption
10 product of the first and second precursor layers. A capacitor dielectric
11 layer may be formed over the first electrode and a second capacitor
12 electrode may be formed over the dielectric layer. The various positions
13 for the barrier layer discussed above are also applicable to the present
14 aspect of the invention.

15 In forming the chemisorption product of the first and second
16 precursor layers, the first and second precursor layers may each consist
17 essentially of a monolayer. Further, the first and second precursor layers
18 may each comprise substantially saturated monolayers. The extent of
19 saturation might not be complete and yet the barrier layer will
20 nevertheless provide the desired properties. Thus, substantially saturated
21 may be adequate. The first and second precursor may each consist
22 essentially of only one chemical species. However, as described above,
23 precursors may also comprise more than one chemical species.

1 Preferably, the first precursor is different from the second precursor,
2 although for some barrier layers, the first and second precursor will be
3 the same. Examples of pairs of first and second precursors include:
4 WF_6/NH_3 , $\text{TaCl}_5/\text{NH}_3$, $\text{TiCl}_4/\text{NH}_3$, tetrakis(dimethylamido)titanium/ NH_3 ,
5 ruthenium cyclopentadiene/ H_2O , $\text{IrF}_5/\text{H}_2\text{O}$, organometallic $\text{Pt}/\text{H}_2\text{O}$. It is
6 conceivable that more than one of the preceding pairs may comprise the
7 first and second precursors, but preferably only one of the pairs.
8 Additional alternating first and second precursor layers may be
9 chemisorbed in keeping with the above aspect of the invention to achieve
10 a desired thickness for the barrier layer.

11 Although ALD and/or chemisorbing first and second precursors may
12 be suitable for forming a barrier layer, other methods may also be
13 suitable. Accordingly, a variety of barrier layer forming techniques may
14 be used in combination with techniques to increase electrode surface area
15 to provide enhancement of capacitance per unit area.

16 In another aspect of the invention, a capacitor fabrication method
17 can include forming a first capacitor electrode over a substrate where the
18 first electrode has an inner surface area per unit area and an outer
19 surface area per unit area that are both greater than an outer surface
20 area per unit area of the substrate. One example of obtaining the inner
21 and outer electrode surface areas involves further forming rugged
22 polysilicon over the substrate and forming the first electrode over the
23 rugged polysilicon. The first electrode can also be formed on the

1 rugged polysilicon. The rugged polysilicon can have a surface area per
2 unit area greater than the surface area per unit area of conventionally
3 formed polysilicon that is not converted to rugged polysilicon. A
4 capacitor dielectric layer and a second capacitor electrode may be formed
5 over the first electrode to produce a capacitor construction.

6 The first electrode can comprise TiN, as well as other materials,
7 and may be deposited by ALD, CVD, and perhaps other methods. The
8 rugged polysilicon can be HSG polysilicon and it can also be undoped.
9 Thus, in the present aspect a first electrode may be formed having an
10 outer surface area at least 30% greater the substrate outer surface area.
11 Advantageously, the first electrode need not comprise polysilicon to
12 accomplish the surface area enhancement. Further, it is conceivable that
13 the first electrode can be formed over materials other than rugged
14 polysilicon that provide enhanced surface area compared to the substrate
15 underlying the first electrode.

16 To achieve more preferred first electrode surface area, rugged
17 polysilicon may be formed using a seed density sufficiently small to yield
18 at least some spaced apart grains. Thus, forming subsequent layers of
19 the capacitor does not fill the space between grains so much as to
20 reduce the capacitance enhancement possible with the first electrode of
21 increased surface area. Conventionally, HSG is formed to optimize
22 surface area with very closely positioned grains since a capacitor
23 electrode will consist of the HSG. In the present aspect of the

1 invention, less closely positioned grains may be formed than would
2 provide optimal surface area for rugged or HSG polysilicon since the
3 first electrode can be formed on the polysilicon rather than consist of
4 the polysilicon. The less closely position grains of the invention will
5 provide a greater outer surface area for the first electrode compared to
6 what HSG optimized for surface area would provide to a first electrode
7 formed on optimized HSG. Also, undoped grains of rugged polysilicon
8 may provide the advantage of grain size being smaller than for doped
9 grains such that a smaller capacitor container may be used.

10 Figs. 1-6 exemplify the features of the various aspects of the
11 invention described above, as well as other aspects of the invention. For
12 example, according to another aspect of the invention, Fig. 1 shows
13 wafer portion 1 including a substrate 2 with an insulative layer 4 formed
14 thereon. A capacitor fabrication method may include forming an opening
15 16 in insulative layer 4, the opening 16 having sides and a bottom.
16 Although not shown, the opening may expose an electrical contact in
17 substrate 2 for subsequent electrical linking with a capacitor electrode.
18 Turning to Fig. 2, a layer of polysilicon 6 may be formed over the sides
19 and bottom of the opening. Polysilicon layer 6 may then be removed
20 from over the bottom of opening 16 and converted by low density
21 seeding to an undoped rugged layer 8 comprising HSG polysilicon, as
22 shown in Fig. 3. An anisotropic spacer etch may be used to remove
23 polysilicon, preferably before conversion, from over the bottom of the

opening while leaving polysilicon over the sides. Accordingly, no undoped polysilicon will exist between an electrical contact, such as a polysilicon or metal plug, in substrate 2 and a bottom capacitor electrode. If polysilicon is present at the bottom, it may cause high contact resistance or an open between the bottom electrode and the contact.

In Fig. 4, a first capacitor electrode 10 may be conformally formed on undoped polysilicon 8. First electrode 10 may be sufficiently thin that it has an outer surface area per unit area greater than an outer surface area per unit area of the portion of substrate 2 underlying first electrode 10. For example, first electrode 10 may have a thickness of from about 50 to about 500 Angstroms, preferably about 200 Angstroms. A capacitor dielectric layer 12 may be formed on first electrode 10 as shown in Fig. 5. Fig. 6 shows excess portions of dielectric layer 12 and a subsequently formed second capacitor electrode layer 14 removed from over insulative layer 4 to produce a capacitor construction.

Advantageously, first electrode 10 has an enhanced surface area yet might not produce a SiO_2 interfacial dielectric with an oxygen containing dielectric layer since first electrode 10 may comprise materials other than polysilicon, for example, TiN. Accordingly, the benefits of high K dielectrics, such as Ta_2O_5 , may be maximized while still providing enhanced electrode surface area.

1 Figs. 7-10 exemplify the features of the various aspects of the
2 invention described above pertaining to barrier layers, as well as other
3 aspects of the invention, according to an alternative process flow. For
4 example, Fig. 7 shows wafer portion 1 of Fig. 2 including a substrate 2
5 with insulative layer 4, opening 16 in insulative layer 4, and polysilicon
6 layer 6 converted to a first capacitor electrode 18 comprising doped HSG
7 polysilicon.

8 In Fig. 8, a conductive barrier layer 20 may be conformally formed
9 on first electrode 18 by, for example, ALD. A capacitor dielectric layer
10 22 may be formed on barrier layer 20. The barrier layer may be
11 sufficiently thick and dense to reduce oxidation of electrode 18 by
12 oxygen diffusion from over the barrier layer. One source of oxygen
13 diffusion may be dielectric layer 22. Fig. 9 shows formation of a second
14 capacitor electrode 24 on dielectric layer 22. Fig. 10 shows excess
15 portions of barrier layer 20, dielectric layer 22, and second electrode
16 layer 24 removed from over insulative layer 4 to form a capacitor
17 construction. As described above, a barrier layer may also be formed
18 over a dielectric layer although not shown in the Figures.

19 In a still further alternative aspect of the invention, barrier layer
20 20 may be removed from over insulative layer 4 prior to forming
21 dielectric layer 22. Chemical mechanical polishing is one example of a
22 suitable removal method for excess portions of barrier layer 20.
23 However, such an alternative is less preferred since the portion of first

1 electrode 18 planar with insulative layer 4 might be exposed during
2 polishing and may contact dielectric layer 22. At the point of contact,
3 an SiO₂ interfacial dielectric may form if first electrode 18 includes
4 silicon and dielectric layer 22 includes oxygen.

5 In compliance with the statute, the invention has been described
6 in language more or less specific as to structural and methodical
7 features. It is to be understood, however, that the invention is not
8 limited to the specific features shown and described, since the means
9 herein disclosed comprise preferred forms of putting the invention into
10 effect. The invention is, therefore, claimed in any of its forms or
11 modifications within the proper scope of the appended claims
12 appropriately interpreted in accordance with the doctrine of equivalents.
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CLAIMS:

1. A capacitor fabrication method comprising:
forming a first capacitor electrode over a substrate;
atomic layer depositing a conductive barrier layer to oxygen diffusion over the first electrode;
forming a capacitor dielectric layer over the first electrode; and
forming a second capacitor electrode over the dielectric layer.
2. The method of claim 1 wherein the atomic layer depositing occurs at a temperature of from about 100 to about 600 °C and at a pressure of from about 0.1 to about 10 Torr.
3. The method of claim 1 wherein the atomic layer deposited barrier layer has a thickness of from about 50 to about 500 Angstroms.
4. The method of claim 1 wherein the atomic layer deposited barrier layer contacts one of the first or second electrodes.
5. The method of claim 1 wherein the atomic layer deposited barrier layer comprises WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys, Ir, Ir alloys, Pd, Pd alloys, RuO_x, or IrO_x.

1 6. The method of claim 1 wherein the dielectric layer exhibits
2 a K factor of greater than about 7 at 20 °C.

3
4 7. The method of claim 1 wherein at least one of the first or
5 second electrodes comprise polysilicon and the dielectric layer comprises
6 oxygen.

7
8 8. The method of claim 1 wherein the dielectric layer comprises
9 Ta₂O₅, ZrO₂, WO₃, Al₂O₃, HfO₂, barium strontium titanate, or strontium
10 titanate.

11
12 9. The method of claim 1 wherein the dielectric layer is over
13 the barrier layer.

14
15 10. The method of claim 9 further comprising atomic layer
16 depositing another conductive barrier layer to oxygen diffusion over the
17 dielectric layer.

18
19 11. The method of claim 1 wherein the forming the electrodes
20 and the dielectric layer occur by other than atomic layer deposition.

1 12. The method of claim 1 further comprising cleaning the first
2 electrode prior to the atomic layer depositing by a method comprising
3 HF dip, HF vapor clean, or NF_3 remote plasma.
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1 13. A capacitor fabrication method comprising:
2 forming a first capacitor electrode over a substrate;
3 chemisorbing a layer of a first precursor at least one monolayer
4 thick over the first electrode;
5 chemisorbing a layer of a second precursor at least one monolayer
6 thick on the first precursor layer, a chemisorption product of the first
7 and second precursor layers being comprised by a layer of a conductive
8 barrier material;
9 forming a capacitor dielectric layer over the first electrode; and
10 forming a second capacitor electrode over the dielectric layer.

11
12 14. The method of claim 13 wherein the first and second
13 precursor layers each consist essentially of a monolayer.

14
15 15. The method of claim 13 wherein the first and second
16 precursor layers each comprise substantially saturated monolayers.

17
18 16. The method of claim 13 wherein the first and second
19 precursor each consist essentially of only one chemical species.

20
21 17. The method of claim 13 wherein the first precursor is
22 different from the second precursor.
23

1 18. The method of claim 13 wherein the first and second
2 precursors respectively comprise only one of the following pairs:
3 WF_6/NH_3 , $\text{TaCl}_5/\text{NH}_3$, $\text{TiCl}_4/\text{NH}_3$, tetrakis(dimethylamido)titanium/ NH_3 ,
4 ruthenium cyclopentadiene/ H_2O , $\text{IrF}_5/\text{H}_2\text{O}$, organometallic $\text{Pt}/\text{H}_2\text{O}$.

5
6 19. The method of claim 13 wherein the dielectric layer is over
7 the barrier layer, further comprising chemisorbing additional alternating
8 first and second precursor layers before forming the dielectric layer.

9
10 20. The method of claim 19 wherein the barrier layer has a
11 thickness and a density effective to reduce oxidation of the first
12 electrode by oxygen from over the barrier layer.

13
14 21. The method of claim 19 wherein the barrier layer has a
15 thickness of from about 50 to about 500 Angstroms.

16
17 22. The method of claim 13 wherein the barrier layer comprises
18 WN , WSiN , TaN , TiN , TiSiN , Pt , Pt alloys, Ir , Ir alloys, Pd , Pd alloys,
19 RuO_x , or IrO_x .

20
21 23. The method of claim 13 wherein the dielectric layer exhibits
22 a K factor of greater than about 7 at 20 °C.
23

1 24. The method of claim 13 wherein at least one of the first or
2 second electrodes comprises polysilicon and the dielectric layer comprises
3 oxygen.

4
5 25. The method of claim 13 wherein the dielectric layer
6 comprises Ta₂O₅, ZrO₂, WO₃, Al₂O₃, HfO₂, barium strontium titanate, or
7 strontium titanate.

1 26. A capacitor construction comprising a first capacitor electrode
2 over a substrate, a capacitor dielectric layer over the first electrode, a
3 second capacitor electrode over the dielectric layer, and an atomic layer
4 deposited conductive barrier layer to oxygen diffusion between the first
5 and second electrodes.

6
7 27. The construction of claim 26 wherein the dielectric layer is
8 over the barrier layer.

9
10 28. The construction of claim 27 further comprising another
11 conductive barrier layer to oxygen diffusion over the dielectric layer.

12
13 29. The construction of claim 26 wherein the barrier layer
14 comprises WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys, Ir, Ir alloys, Pd,
15 Pd alloys, RuO_x, or IrO_x.

16
17 30. The construction of claim 26 wherein the dielectric layer
18 exhibits a K factor of greater than about 7 at 20 °C.

1 31. A capacitor construction comprising:
2 a first capacitor electrode over a substrate;
3 a conductive barrier layer to oxygen diffusion over the first
4 electrode, the barrier layer comprising a chemisorption product of first
5 and second precursor layers;
6 a capacitor dielectric layer over the first electrode; and
7 a second capacitor electrode over the dielectric layer.

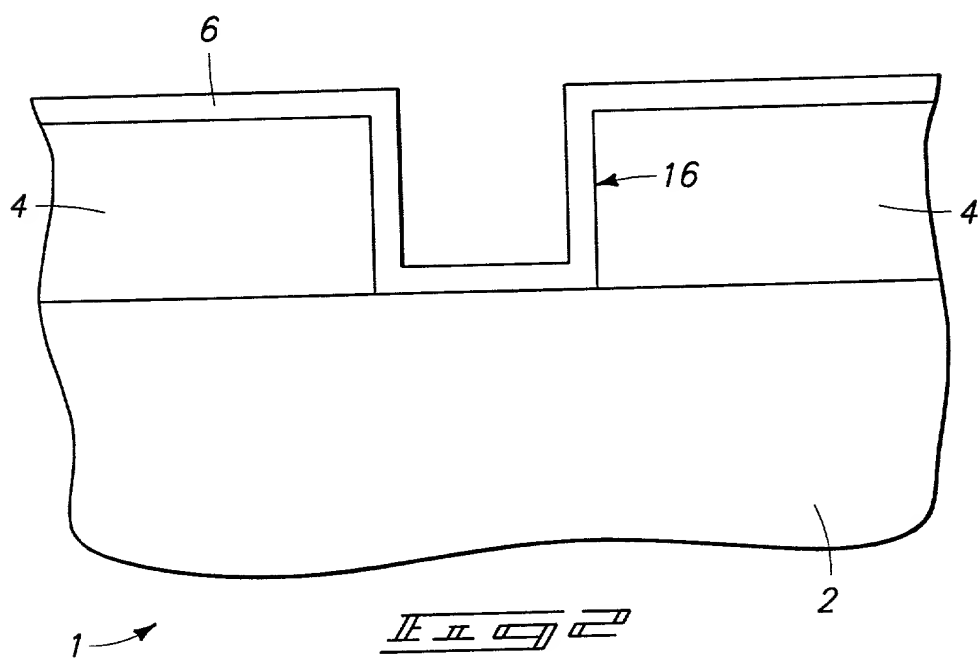
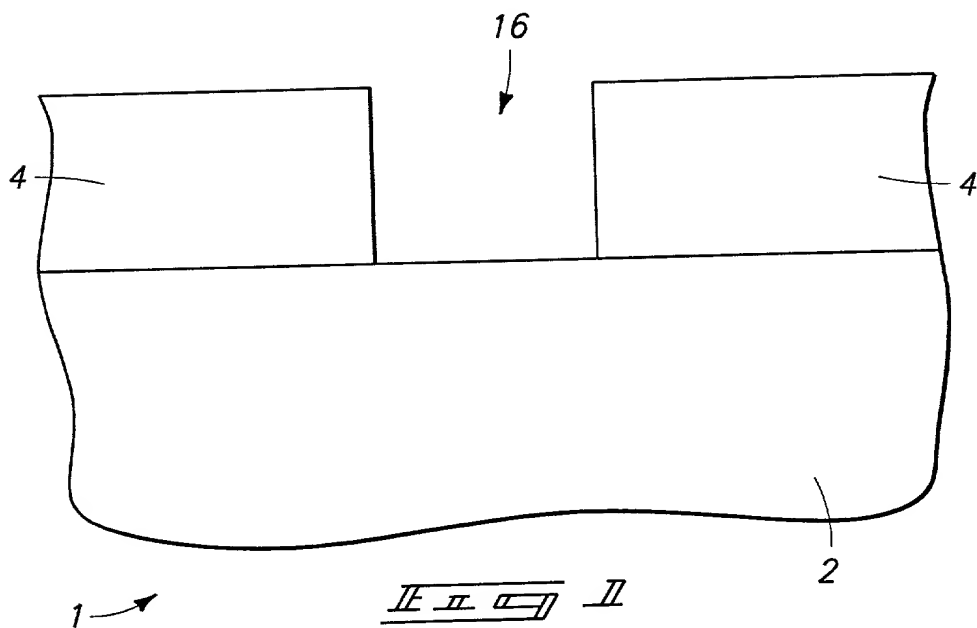
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9 32. The construction of claim 31 wherein the barrier layer
10 comprises WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys, Ir, Ir alloys, Pd,
11 Pd alloys, RuO_x, or IrO_x.

12
13 33. The construction of claim 31 wherein the dielectric layer
14 exhibits a K factor of greater than about 7 at 20 °C.
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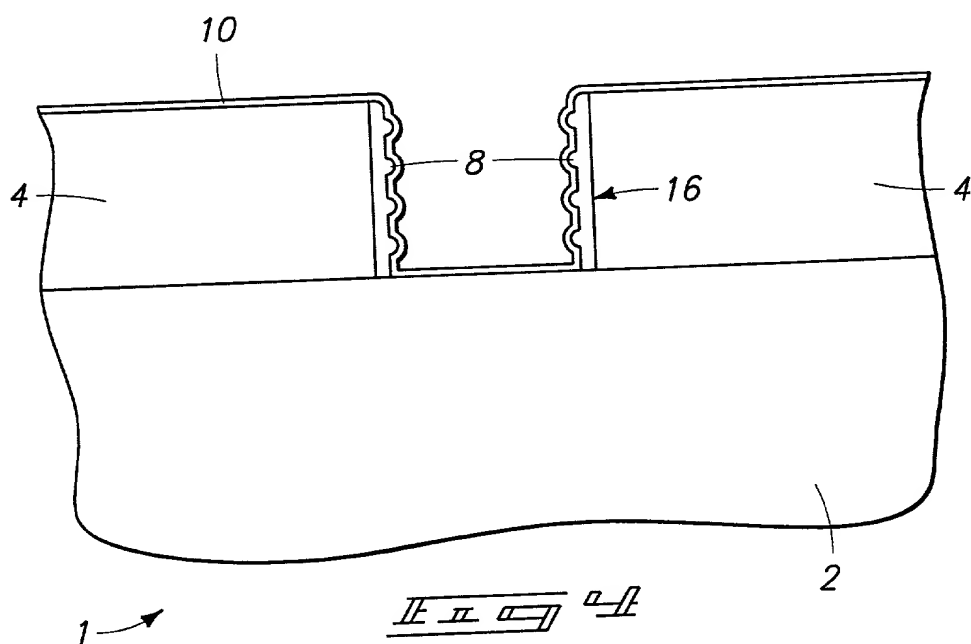
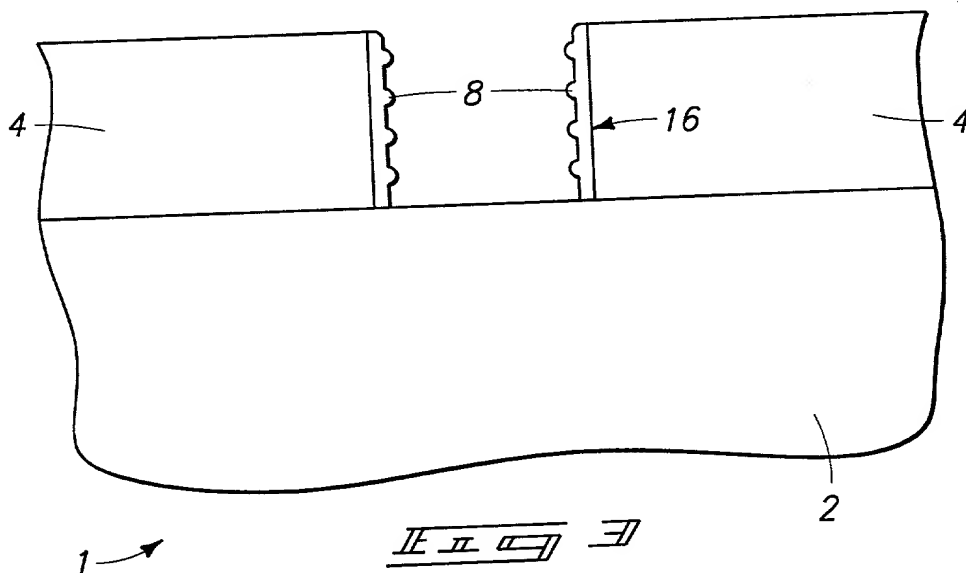
1 **ABSTRACT OF THE DISCLOSURE**

2 A capacitor fabrication method may include atomic layer depositing
3 a conductive barrier layer to oxygen diffusion over the first electrode.
4 A method may instead include chemisorbing a layer of a first precursor
5 at least one monolayer thick over the first electrode and chemisorbing
6 a layer of a second precursor at least one monolayer thick on the first
7 precursor layer, a chemisorption product of the first and second
8 precursor layers being comprised by a layer of a conductive barrier
9 material. The barrier layer may be sufficiently thick and dense to
10 reduce oxidation of the first electrode by oxygen diffusion from over the
11 barrier layer. An alternative method may include forming a first
12 capacitor electrode over a substrate, the first electrode having an inner
13 surface area per unit area and an outer surface area per unit area that
14 are both greater than an outer surface area per unit area of the
15 substrate. A capacitor dielectric layer and a second capacitor electrode
16 may be formed over the dielectric layer. The method may further
17 include forming rugged polysilicon over the substrate, the first electrode
18 being over the rugged polysilicon. Accordingly, the outer surface area
19 of the first electrode can be at least 30% greater than the outer surface
20 area of the substrate without the first electrode including polysilicon.

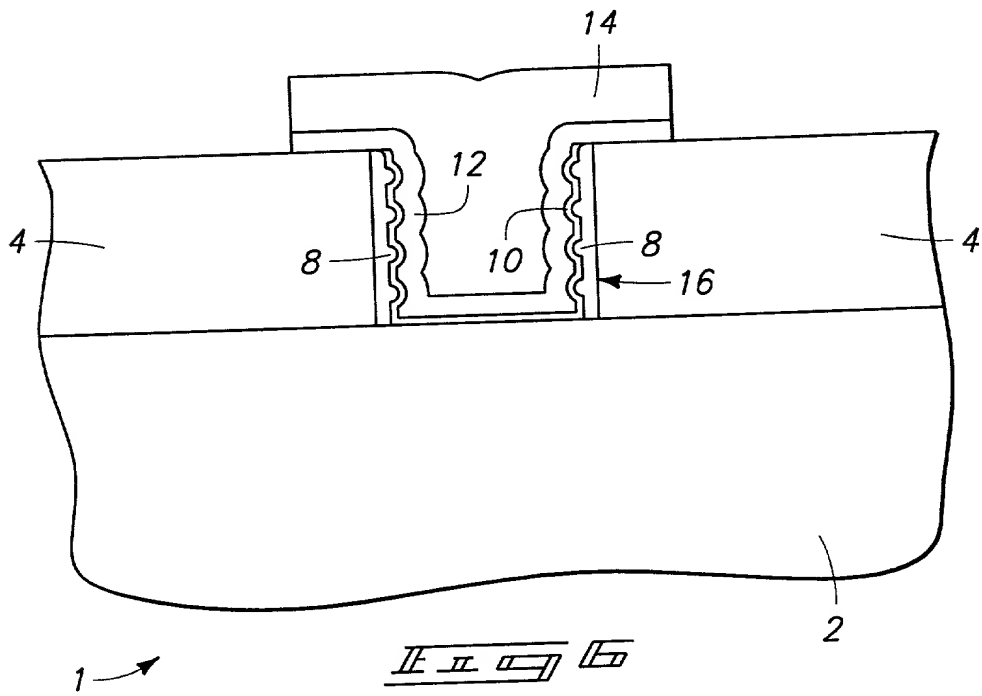
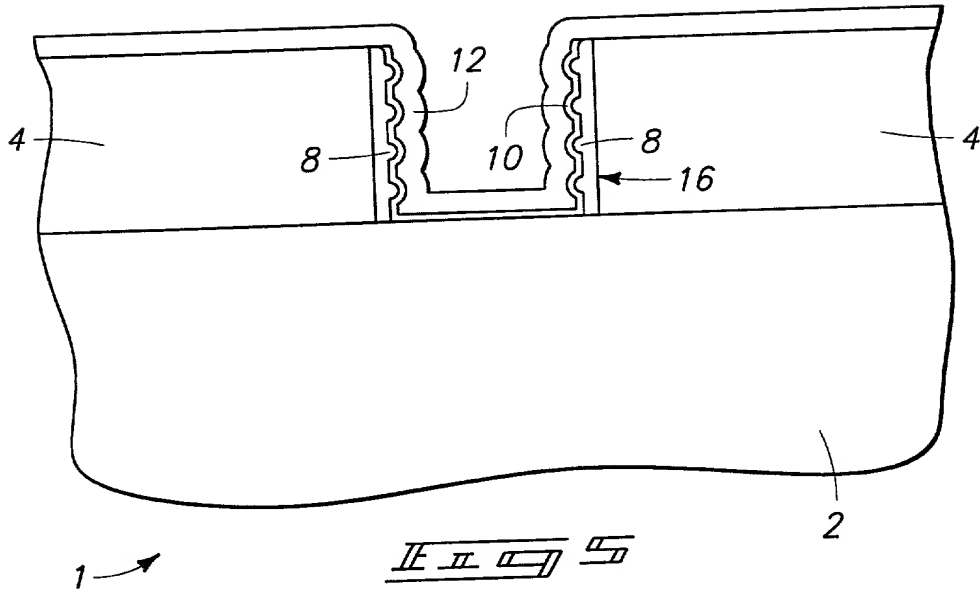
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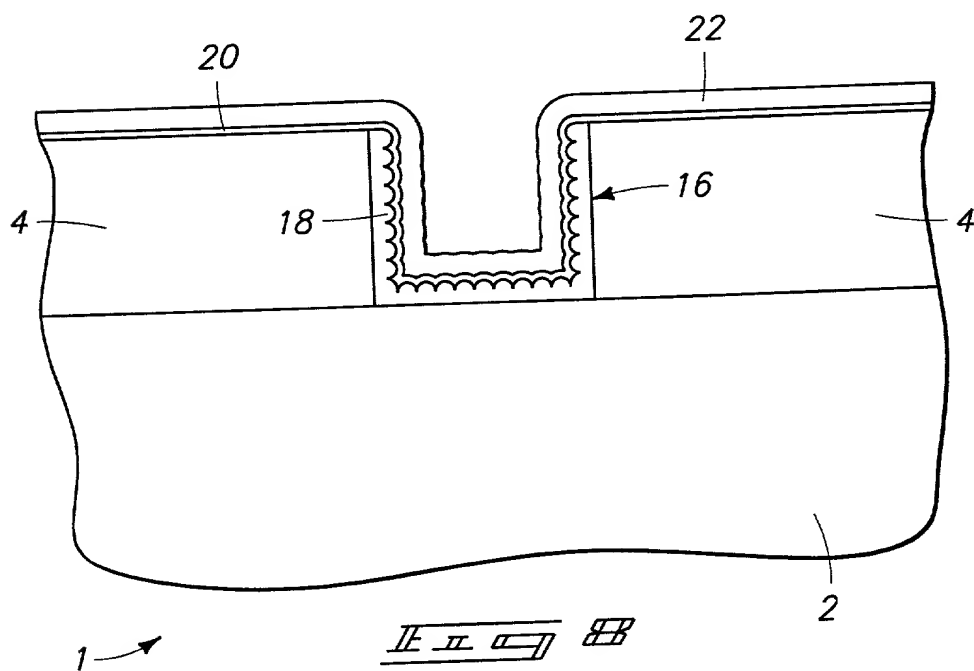
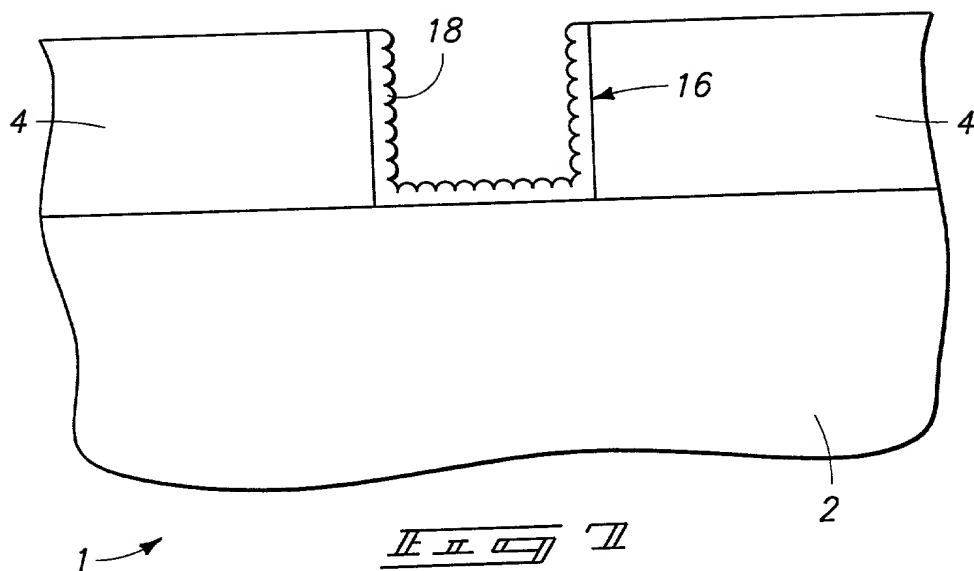
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